Towards an Ultra-Low-Power Architecture Using Single-Electron Tunneling Transistors

Queen's University
Changyun Zhu
Li Shang
Robert Knobel

Northwestern University
Zhenyu Gu
Robert Dick

6 June 2007
Executive Summary

Motivation
- CMOS is approaching fabrication, power, and thermal limits
- Can new device technologies solve these problems?

Single electron tunneling transistor (SET)
- Unique property: lowest projected power consumption
- Challenges: fabrication for room-temperature operation, offset charge noise, etc.

Goal: investigate possible uses of SETs in low-power design
- IceFlex: fault-tolerant, SET/CMOS reconfigurable architecture
- $100\times$ energy efficiency improvement over 22 nm CMOS
- Designed for unique challenges posed by SETs
Introduction
  - Power, energy, and thermal challenges

Background
  - SET properties and challenges

Testbed design
  - IceFlex: a hybrid SET/CMOS reconfigurable architecture

Evaluation
  - Possible uses of SETs in low-power design

Conclusions
Power challenges

High-performance applications: energy cost, temperature, reliability
Portable embedded systems: battery lifetime

![Graph showing the power consumption of various processors over time.](image)
What does history teach us about power consumption?

Device innovations have been the most effective method:
- Vacuum tube to semiconductor device in the 1960s
- Bipolar device to CMOS transistor in the 1990s

Based on diagram by C. Johnson, IBM Server and Technology Group.
Single electron tunneling transistor structure

Device structure
- Island, terminals (source, drain, gate)
- Electron tunneling through tunneling junctions

C<sub>G</sub>: gate capacitance
C<sub>G2</sub>: optional 2<sup>nd</sup> gate capacitance
C<sub>S</sub>: source tunnel junction capacitance
R<sub>S</sub>: source tunnel junction resistance
R<sub>D</sub>: drain tunnel junction resistance
C<sub>D</sub>: drain tunnel junction capacitance

Diagram showing the structure with labels and symbols for the components.
Single electron tunneling transistor behavior

Physical principles

- Coulomb charging effect governs electron tunneling
- Coulomb blockade \( V_{GS} = \frac{me}{C_G} \), \( m = \pm \frac{1}{2}, \pm \frac{3}{2}, \cdots \) OFF, \( m = 0, \pm 1, \pm 2, \cdots \) ON
SET properties and challenges

Ultra low power
- Projected energy per switching event \( (1 \times 10^{-18} \text{ J}) \)

Room temperature and fabrication challenge
- Electrostatic charging energy must be greater than thermal energy
- \( \frac{e^2}{C_\Sigma} > k_B T \)
- Requires \( \frac{e^2}{C_\Sigma} > 10k_B T \) or even \( \frac{e^2}{C_\Sigma} > 40k_B T \)
SET properties and challenges

Performance challenge

- Electrons must be confined in the island
- \( R_S, R_D > \frac{h}{e^2}, \frac{h}{e^2} = 25.8 \, \text{k}\Omega \)
- High resistance, low driving strength

Reliability concerns

- Tunneling between charge traps cause run-time errors
- Unknown before fabrication
- Device technology: Improved by silicon islands
- Reliable design: Post-fabrication adaptation
- Run-time error correction
IceFlex: low-power, fault-tolerant, hybrid SET/CMOS reconfigurable architecture

Goal
Develop a testbed to investigate possible uses of SETs in low-power embedded system design

Design metrics
Power consumption, performance, reliability, fabrication, cooling

SET-specific design features
- Fabrication challenge: Regular architecture to ease fabrication
- Reliability challenge: Built-in redundancy, fault-tolerant design
- Performance challenge: Hybrid SET/CMOS design
- Unique properties: Multi-gate design for non-linearly-separable functions and voting logic
IceFlex architecture

Fault-tolerant, hybrid SET/CMOS reconfigurable architecture

- Multi-gate SET-based reconfigurable look-up tables and switch fabric
- SET-based arithmetic unit
- SET-based reconfiguration memory
- SET threshold logic-based majority voting logic
- Hybrid SET/CMOS multi-level interconnect fabric
Multi-gate SET reconfigurable lookup table

SET multi-gate integration

- Gate charging effect: a function of $\sum C_{Gi} V_{GSi}$
- Multiplexer design: reduce logic depth, hence circuit delay

m-to-1 multi-gate multiplexer SET tree

$m_c$-to-1 multi-gate SET multiplexer
Multi-context on-chip storage design

- Multi-context configuration cache
- Dual-island SET design

SET configuration memory

Configuration sets:
- set k-1
- set1
- set0

Store 1
- charge

Store 0

SET memory cell
Efficient SET arithmetic function

**SET non-unate logic**
- Complicated design using threshold logic, BJT, and CMOS
- Taking advantage of the periodic nature of SET I–V characteristics
Interconnect

Local interconnect
- Requires limited driving strength
- Constant-latency, SET-based design
- Simplify physical design, i.e., routing

Global interconnect
- Requires high driving strength
- Hybrid SET/CMOS design

![Inter-HLB metal wire circuit diagram]
Potential uses of single-electron tunneling transistors

**Application domains**
- High-performance applications
- Battery-powered systems

**Design metrics**
- Power, performance
- Fabrication, reliability

<table>
<thead>
<tr>
<th>Benchmarks</th>
<th>Description</th>
<th>Benchmarks</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>AES</td>
<td>AES (Rijndael) IP core</td>
<td>ARM7</td>
<td>Power-efficient RISC CPU</td>
</tr>
<tr>
<td>AVR</td>
<td>ATMega103 microcontroller</td>
<td>ASPIDA DLX</td>
<td>Synchronous / DLX core</td>
</tr>
<tr>
<td>CORDIC</td>
<td>Coordinate rotation computer</td>
<td>Jam RISC</td>
<td>Five-stage pipeline RISC CPU</td>
</tr>
<tr>
<td>ECC</td>
<td>ECC core</td>
<td>LEON2 SPARC</td>
<td>Entire SPARC V8 processor</td>
</tr>
<tr>
<td>FPU</td>
<td>32-bit IEEE 754 floating-point</td>
<td>Microblaze</td>
<td>RISC CPU</td>
</tr>
<tr>
<td>RS</td>
<td>Reed Solomon encoder</td>
<td>miniMIPS</td>
<td>MIPS I clone</td>
</tr>
<tr>
<td>USB</td>
<td>USB 2.0 function</td>
<td>MIPS</td>
<td>MIPS processor</td>
</tr>
<tr>
<td>VC</td>
<td>Video compression systems</td>
<td>Plasma</td>
<td>Supports most MIP I opcodes</td>
</tr>
<tr>
<td>UCore</td>
<td>MIPS I integer only clone</td>
<td>YACC</td>
<td>MIPS I clone</td>
</tr>
</tbody>
</table>
SET-based design can improve system energy efficiency by 100×.
IceFlex optimized for battery-powered applications

Non-redundant battery powered-10KBT
Redundant battery powered-10KBT
Non-redundant battery powered-40KBT
Redundant battery powered-40KBT
## Room-temperature operation, cooling, and fabrication

<table>
<thead>
<tr>
<th>Temperature (K)</th>
<th>CMOS operation</th>
<th>4.65</th>
<th>52.48</th>
<th>1.16</th>
<th>13.12</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Liquid nitrogen cooling</td>
<td>2.41</td>
<td>27.26</td>
<td>0.60</td>
<td>6.82</td>
</tr>
<tr>
<td></td>
<td>Average cloud top temp.</td>
<td>1.80</td>
<td>20.38</td>
<td>0.45</td>
<td>5.10</td>
</tr>
<tr>
<td></td>
<td>Cryogenic</td>
<td>1.55</td>
<td>17.49</td>
<td>0.39</td>
<td>4.37</td>
</tr>
<tr>
<td></td>
<td>SET device</td>
<td>0.93</td>
<td>10.50</td>
<td>0.23</td>
<td>2.62</td>
</tr>
<tr>
<td></td>
<td>Stacked Peltier heat pump</td>
<td>0.74</td>
<td>8.40</td>
<td>0.19</td>
<td>2.10</td>
</tr>
<tr>
<td></td>
<td>Room temperature</td>
<td>0.62</td>
<td>7.00</td>
<td>0.15</td>
<td>1.75</td>
</tr>
</tbody>
</table>

### Observations
- Nanometer-scale fabrication to enable room-temperature operation
- Compact cooling design at cryogenic temperature range
Reliability

Impact of Majority Voting Logic

- MVL can significantly minimize circuit failures
- IceFlex supports Run-time failure detect and correction

<table>
<thead>
<tr>
<th>Majority vote inputs</th>
<th>SET fault probability</th>
<th>Raw fail prob.</th>
<th>SET MVL prob.</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>1/10,000</td>
<td>1/157</td>
<td>1/8,200</td>
</tr>
<tr>
<td>5</td>
<td></td>
<td>1/157</td>
<td>1/372,000</td>
</tr>
<tr>
<td>7</td>
<td></td>
<td></td>
<td>1/5,650,000</td>
</tr>
</tbody>
</table>

Recent advances in device technology may greatly reduce error rate.

Assume many-core systems can be efficiently used in the future
Given 100 W power budget
Supports approximately 4,500 LEON2 SPARC cores at 1 GHz
Approximately 4.8 Terra instructions per second
Case study: Battery-powered applications

Given one AA battery
IceFlex AVR can run 20 years

Given 5 cm$^3$ scavenging volume
- Can run at max frequency from vibrations (200 µW/cm$^3$)
- Max frequency from temperature variations (10 µW/cm$^3$)
- 3.7 MHz from indoor solar energy (4 µW/cm$^3$)
- 2.8 kHz from 75 dB acoustic noise (0.003 µW/cm$^3$)

Conclusions

Investigated potential of SETs in low-power system design

Designed IceFlex, a low-power, fault-tolerant, hybrid SET/CMOS reconfigurable architecture

Opportunities and challenges

- Orders of magnitude power and energy efficiency improvement
- Fabrication, cooling design, and reliability challenges